

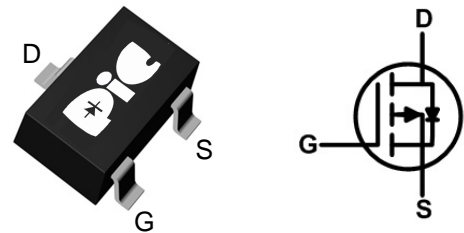
➤ General Description

This PAP2617N P-Channel enhancement mode power field effect transistor is the high density trench technology and this advanced technology can provide excellent $R_{ds(On)}$ performance and efficiency for power switching and load switching application., this device also comply with the RoHS and Green Product requirement with full function reliability approved.

➤ Feature

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology
- SOT-23 Package design

➤ SOT-23



➤ Application

- Load Switch
- Small Power Switching
- Power Management

➤ Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current, $V_{GS} @ -4.5V^1$	$I_D @ T_A=25^\circ C$	-4.7	A
Continuous Drain Current, $V_{GS} @ -4.5V^1$	$I_D @ T_A=70^\circ C$	-3.8	A
Pulsed Drain Current ²	I_{DM}	-18.8	A
Total Power Dissipation ³	$P_D @ T_A=25^\circ C$	1	W
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ C$
Operating Junction Temperature Range	T_J	-55 to 150	$^\circ C$
Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	125	$^\circ C/W$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	80	$^\circ C/W$

➤ Electrical Characteristics ($T_J=25^\circ C$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to $25^\circ C, I_D=-1mA$	---	-0.01	---	V/ $^\circ C$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-4A$	---	25	32	m Ω
		$V_{GS}=-2.5V, I_D=-2A$	---	32	40	
		$V_{GS}=-1.8V, I_D=-1.5A$	---	42	55	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.3	-0.5	-1.0	V
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}$		---	2.96	---	mV/ $^\circ C$
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V, T_J=25^\circ C$	---	---	-1	uA
		$V_{DS}=-16V, V_{GS}=0V, T_J=55^\circ C$	---	---	-5	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-4A$	---	21	---	S
Total Gate Charge (-4.5V)	Q_g	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-4A$	---	27.3	38.2	nC
Gate-Source Charge	Q_{gs}		---	3.6	5.0	
Gate-Drain Charge	Q_{gd}		---	6.5	9.1	
Turn-On Delay Time	$T_{d(on)}$	$V_{DD}=-10V, V_{GS}=-4.5V, R_G=3.3\Omega, I_D=-4A$	---	9.2	18.4	ns
Rise Time	T_r		---	59	106	
Turn-Off Delay Time	$T_{d(off)}$		---	99	198	
Fall Time	T_f		---	71	142	
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	---	2280	3192	pF
Output Capacitance	C_{oss}		---	220	308	
Reverse Transfer Capacitance	C_{riss}		---	187	262	

➤ Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current ^{1,4}	I_S	$V_G=V_D=0V, \text{ Force Current}$	---	---	-4.7	A
Pulsed Source Current ^{2,4}	I_{SM}		---	---	-18.8	A
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=-1A, T_J=25^\circ C$	---	---	-1	V
Reverse Recovery Time	t_{rr}	$I_F=-4A, di/dt=100A/\mu s, T_J=25^\circ C$	---	52	---	nS
Reverse Recovery Charge	Q_{rr}		---	28	---	nC

Note :

1. Pulse width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. Ensure that the channel temperature does not exceed $150^\circ C$.
4. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

➤ Typical Characteristics

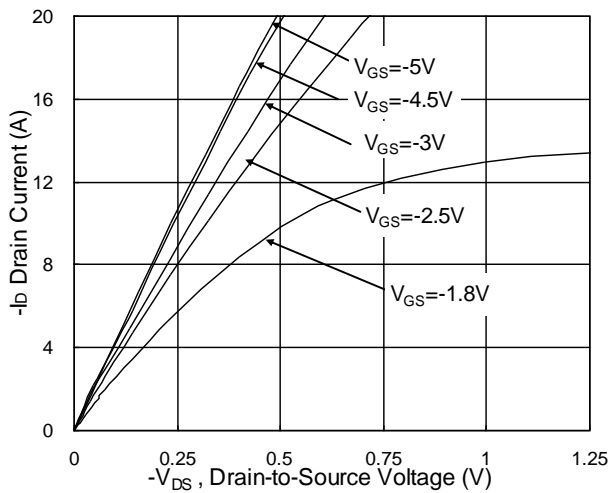


Fig.1 Typical Output Characteristics

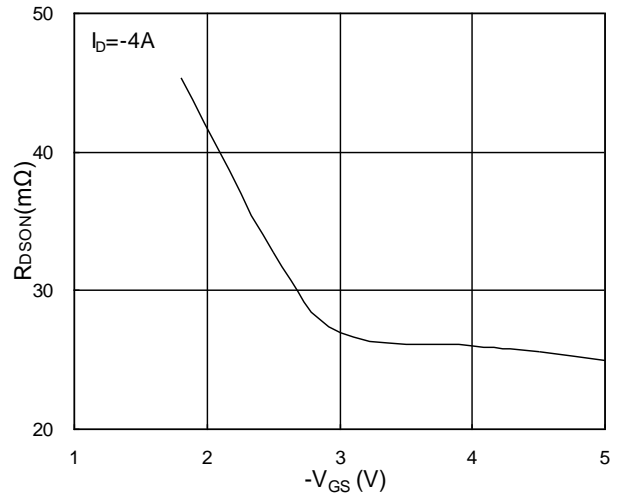


Fig.2 On-Resistance vs. Gate-Source

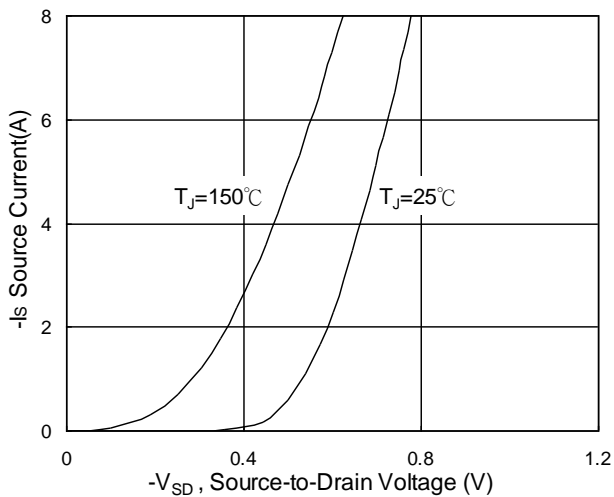


Fig.3 Forward Characteristics Of Reverse

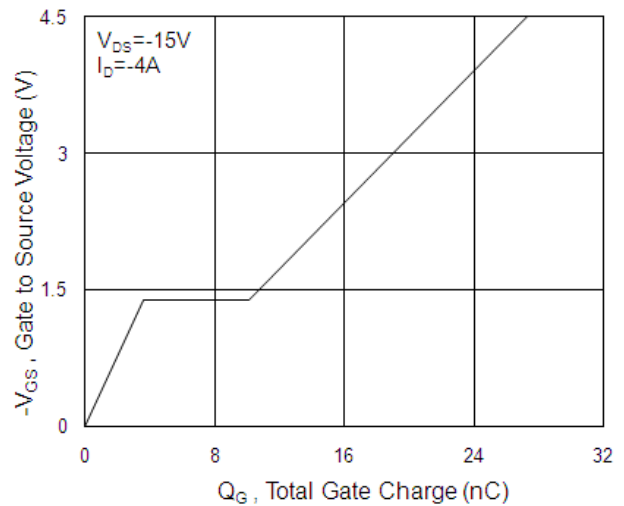


Fig.4 Gate-Charge Characteristics

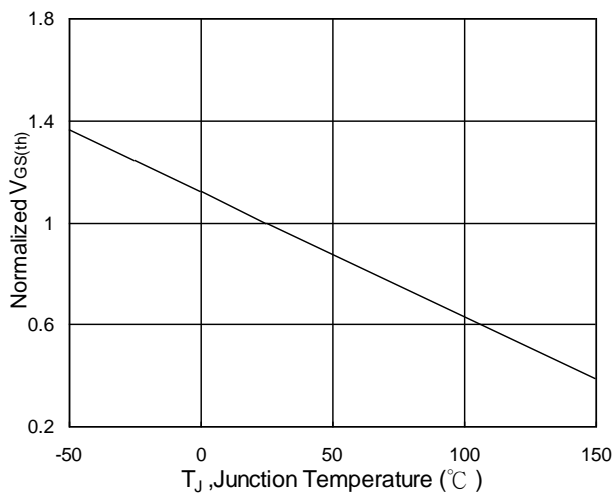


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

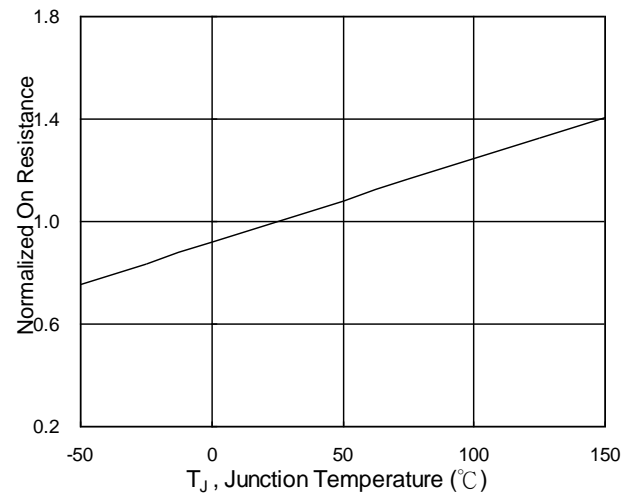


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

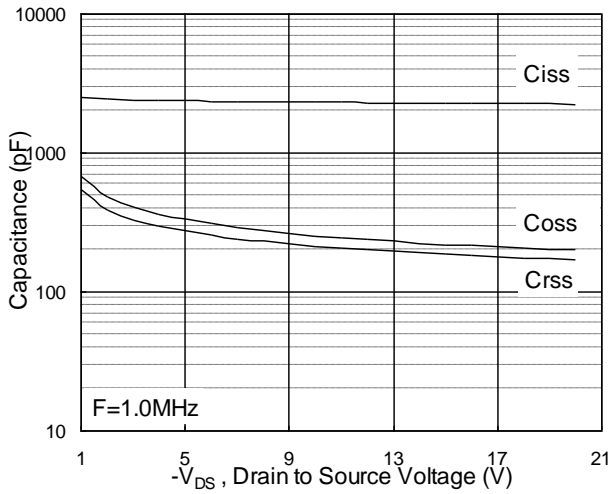


Fig.7 Capacitance

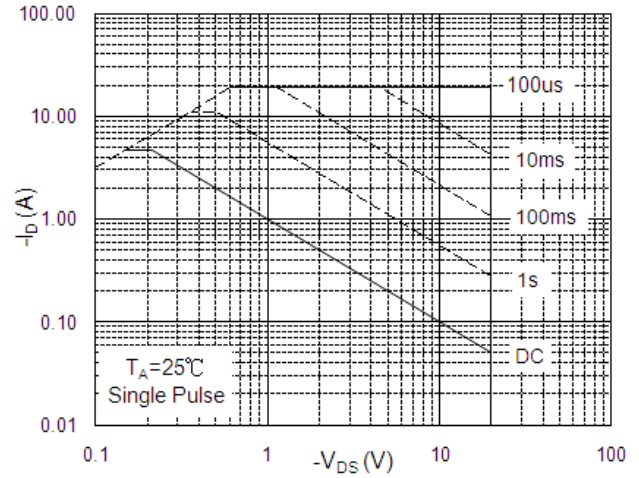


Fig.8 Safe Operating Area

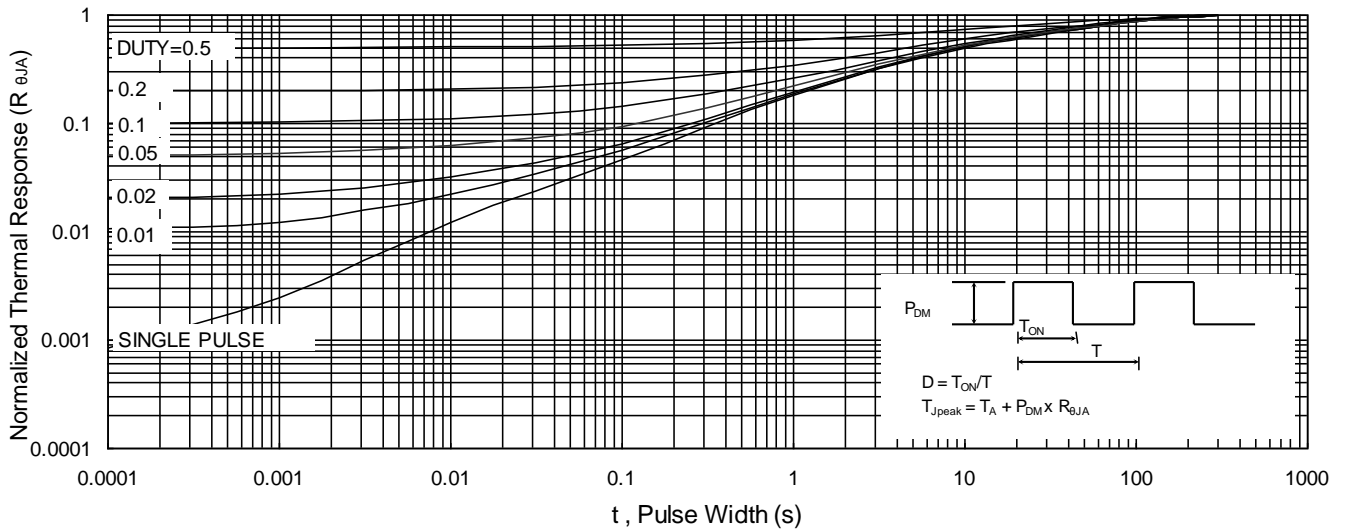


Fig.9 Normalized Maximum Transient Thermal Impedance

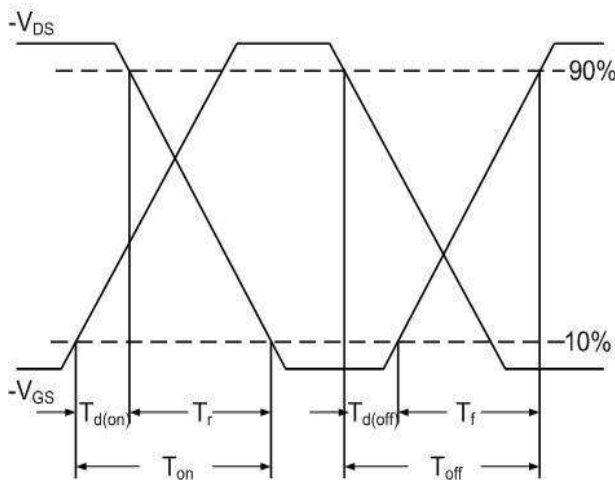


Fig.10 Switching Time Waveform

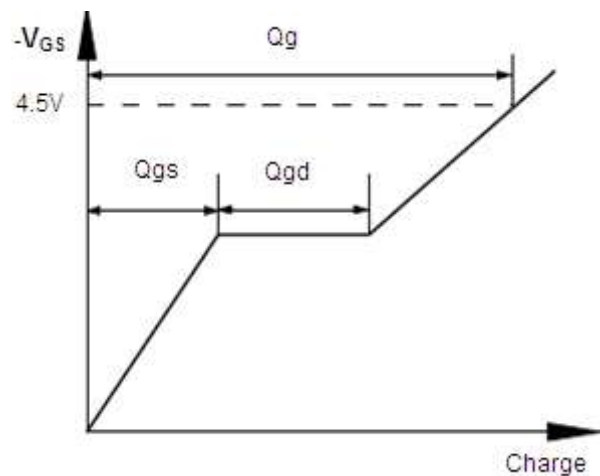
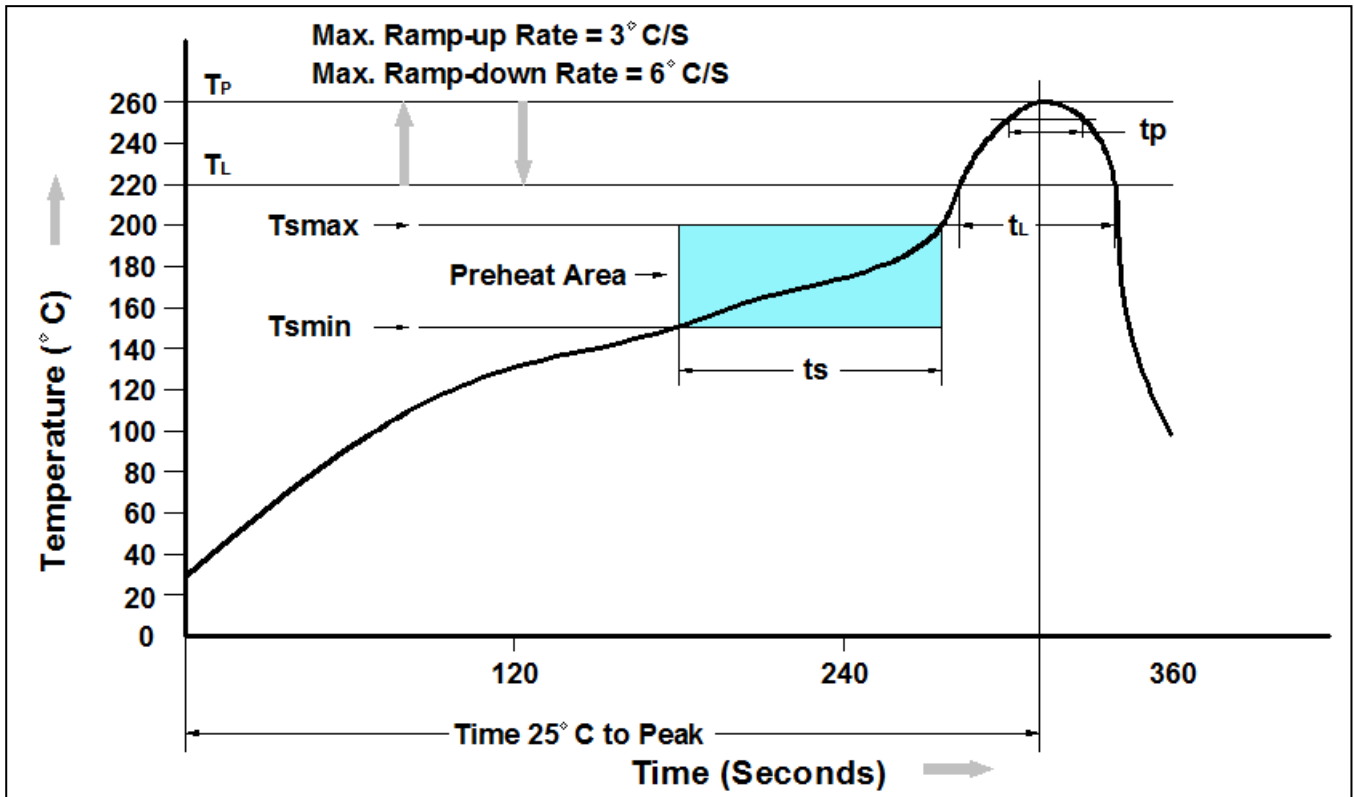


Fig.11 Gate Charge Waveform

➤ Recommand IR Reflow Soldering Thermal Profile

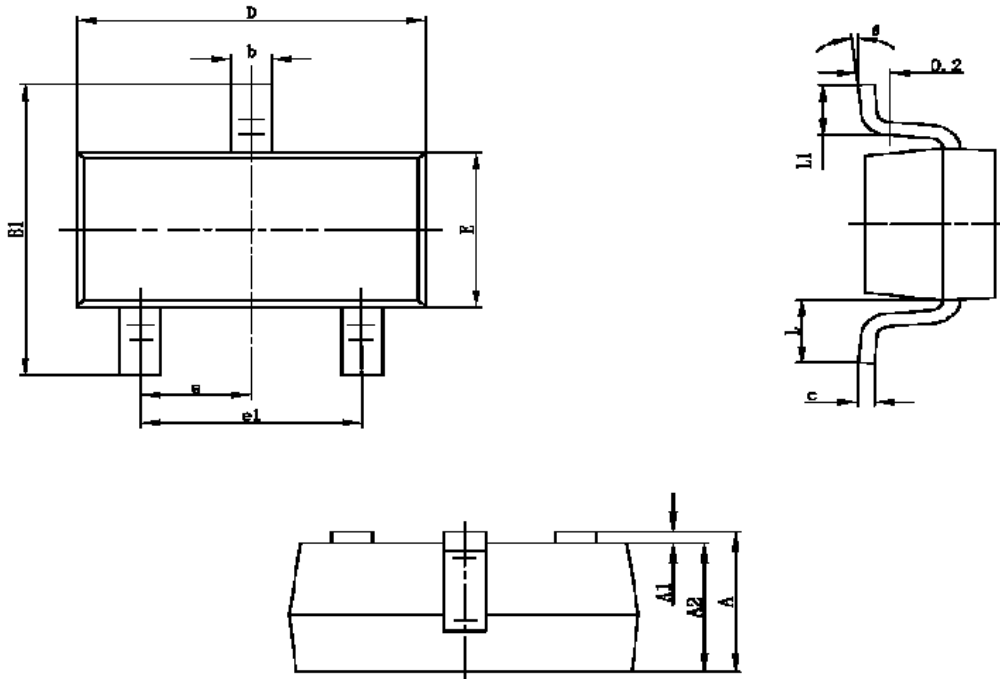


Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T_{smin})	150°C
Temperature Max. (T_{smax})	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds
Average Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Temperature	260°C +0°C / -5°C
Time (t_P) within 5°C of actual Peak Temperature	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.

➤ Ordering Information

Part Number	Description	Quantity
PAP2617N	SOT-23 Reel	3000 pcs

➤ Package Information (SOT-23)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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