PAC49TY03YB

N-Ch and P-Ch Fast Switching MOSFET

V_{DS}=40V, I_D=26A, $RDS_{(ON)}$=30mΩ

V_{DS}=-40V, I_D=-25A, $RDS_{(ON)}$=45mΩ

➢ General Description

This PAC49TY03YB N&P Channel enhancement mode power field effect transistor is the high density trench technology and this advanced technology can provide excellent Rds(On) performance and efficiency for power switching and load switching application., this device also comply with the RoHS and Green Product requirement with full function reliability approved.

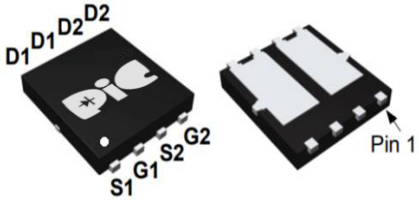
➢ Feature

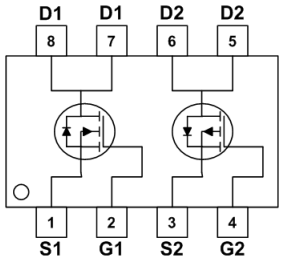
- ●Super Low Gate Charge
- ●100% EAS Guaranteed
- ●Green Device Available
- ●Excellent CdV/dt effect decline
- ●Advanced high cell density Trench technology
- ●DFN5x6A-EP2 package design

➢ Application

- ●DC/DC Primary Side Switch
- ●Industrial Synchronous
- ●Rectification Load Switch
- ●DC/DC Converters

➢ DFN5X6A-EP2





➢ Absolute Maximum Ratings

Parameter	Symbol	Rating		Units
		N-Ch	P-Ch	
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current, V_{GS} @ 10V[1]	I_D@T_C=25℃	26	-25	A
Continuous Drain Current, V_{GS} @ 10V[1]	I_D@T_C=100℃	18	-16	A
Pulsed Drain Current[2]	I_{DM}	47	-46	A
Single Pulse Avalanche Energy[3]	EAS	28	66	mJ
Avalanche Current	I_{AS}	17.8	-27.2	A
Total Power Dissipation[4]	P_D@T_C=25℃	35.7	35.7	W
Storage Temperature Range	T_{STG}	-55 to 150	-55 to 150	℃
Operating Junction Temperature Range	T_J	-55 to 150	-55 to 150	℃
Thermal Resistance Junction-Ambient [1]	$R_{\theta JA}$	---	62	℃/W
Thermal Resistance Junction-Case[1]	$R_{\theta JC}$	---	3.5	℃/W

N-Ch and P-Ch Fast Switching MOSFET

V_{DS}=40V, I_D=26A, $RDS_{(ON)}$=30mΩ

V_{DS}=-40V, I_D=-25A, $RDS_{(ON)}$=45mΩ

➢ N-Channel Electrical Characteristics (TJ=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=250uA	40	---	---	V
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	V_{GS}=10V , I_D=12A	---	---	30	mΩ
		V_{GS}=4.5V , I_D=10A	---	---	50	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=32V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=55℃	---	---	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
Forward Transconductance	gfs	V_{DS}=5V , I_D=12A	---	8	---	S
Total Gate Charge (4.5V)	Q_g	V_{DS}=20V , V_{GS}=4.5V , I_D=12A	---	5.5	---	nC
Gate-Source Charge	Q_{gs}		---	1.25	---	
Gate-Drain Charge	Q_{gd}		---	2.5	---	
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=20V , V_{GS}=10V , R_G=3.3Ω I_D=1A	---	8.9	---	ns
Rise Time	T_r		---	2.2	---	
Turn-Off Delay Time	$T_{d(off)}$		---	41	---	
Fall Time	T_f		---	2.7	---	
Input Capacitance	C_{iss}	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	593	---	pF
Output Capacitance	C_{oss}		---	76	---	
Reverse Transfer Capacitance	C_{rss}		---	56	---	

➢ Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current[1,5]	I_S	V_G=V_D=0V , Force Current	---	---	23	A
Diode Forward Voltage[2]	V_{SD}	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :

1.Pulse width limited by maximum junction temperature.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=17.8A

4.Ensure that the channel temperature does not exceed 150°C.

5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

➢ P-Channel Electrical Characteristics (TJ=25° C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=-250uA	-40	---	---	V
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	V_{GS}=-10V , I_D=-8A	---	---	45	mΩ
		V_{GS}=-4.5V , I_D=-4A	---	---	70	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.6	-2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-32V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-32V , V_{GS}=0V , T_J=55℃	---	---	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
Forward Transconductance	gfs	V_{DS}=-5V , I_D=-8A	---	12.6	---	S
Total Gate Charge (-4.5V)	Q_g	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-12A	---	9	---	nC
Gate-Source Charge	Q_{gs}		---	2.54	---	
Gate-Drain Charge	Q_{gd}		---	3.1	---	
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω, I_D=-1A	---	19.2	---	ns
Rise Time	T_r		---	12.8	---	
Turn-Off Delay Time	$T_{d(off)}$		---	48.6	---	
Fall Time	T_f		---	4.6	---	
Input Capacitance	C_{iss}	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	1004	---	pF
Output Capacitance	C_{oss}		---	108	---	
Reverse Transfer Capacitance	C_{rss}		---	80	---	

➢ Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current[1,5]	I_S	V_G=V_D=0V , Force Current	---	---	-20	A
Diode Forward Voltage[2]	V_{SD}	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V

Note :
1.Pulse width limited by maximum junction temperature.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-27.2A
4.Ensure that the channel temperature does not exceed 150°C.
5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

➢ N-Channel Typical Characteristics

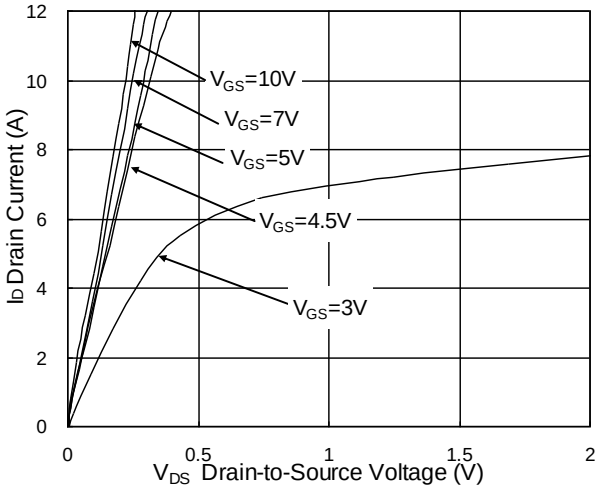


Fig.1 Typical Output Characteristics

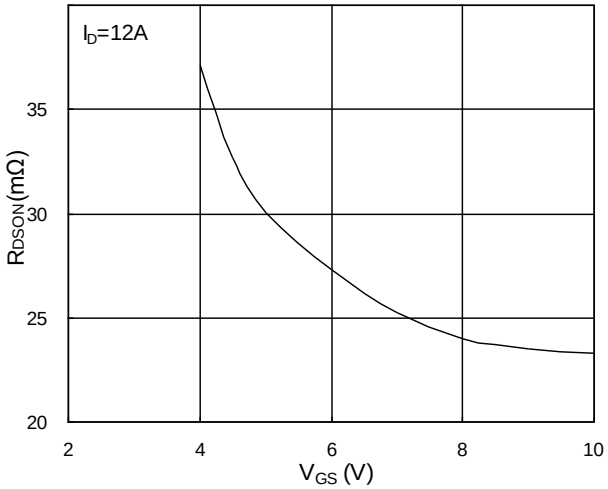


Fig.2 On-Resistance vs. G-S Voltage

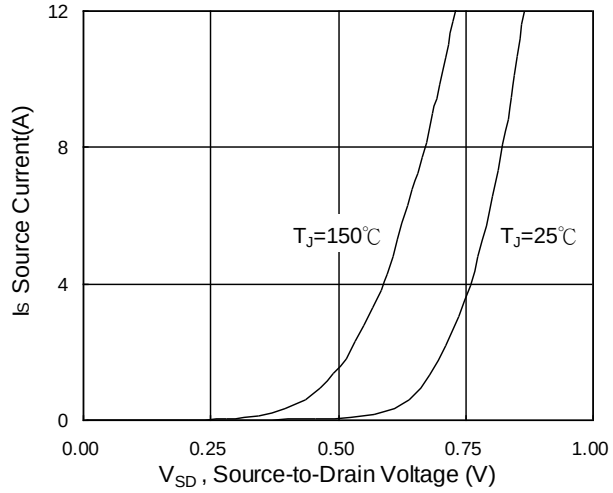


Fig.3 Source Drain Forward Characteristics

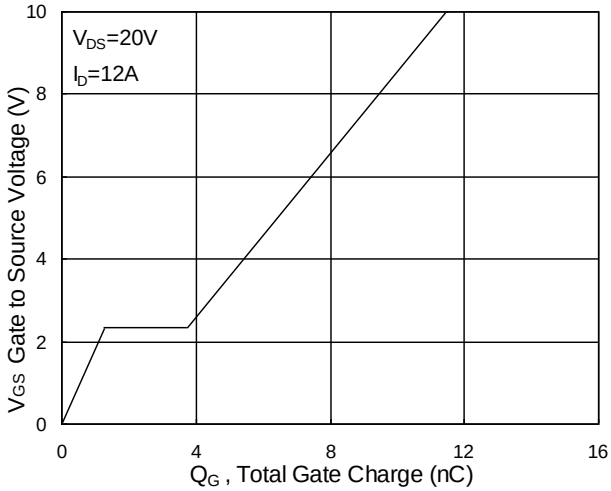


Fig.4 Gate-Charge Characteristics

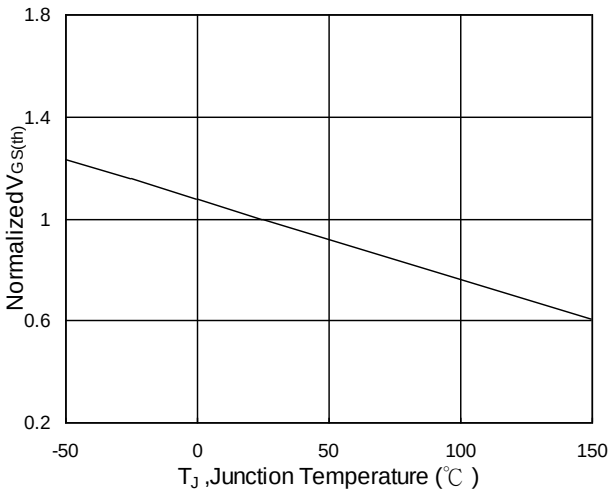


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

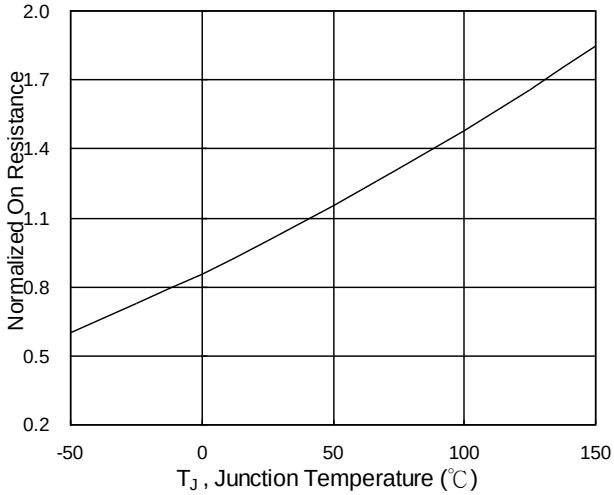


Fig.6 Normalized R_{DSON} vs. T_J

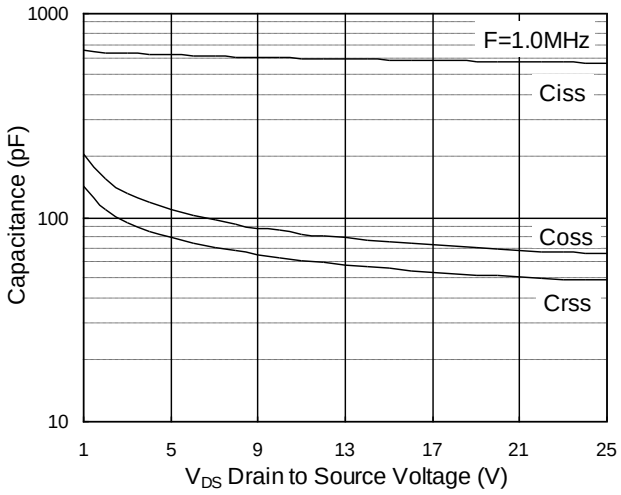


Fig.7 Capacitance

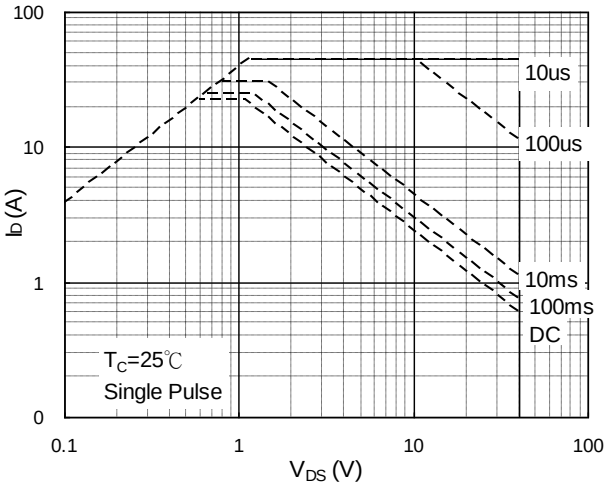


Fig.8 Safe Operating Area

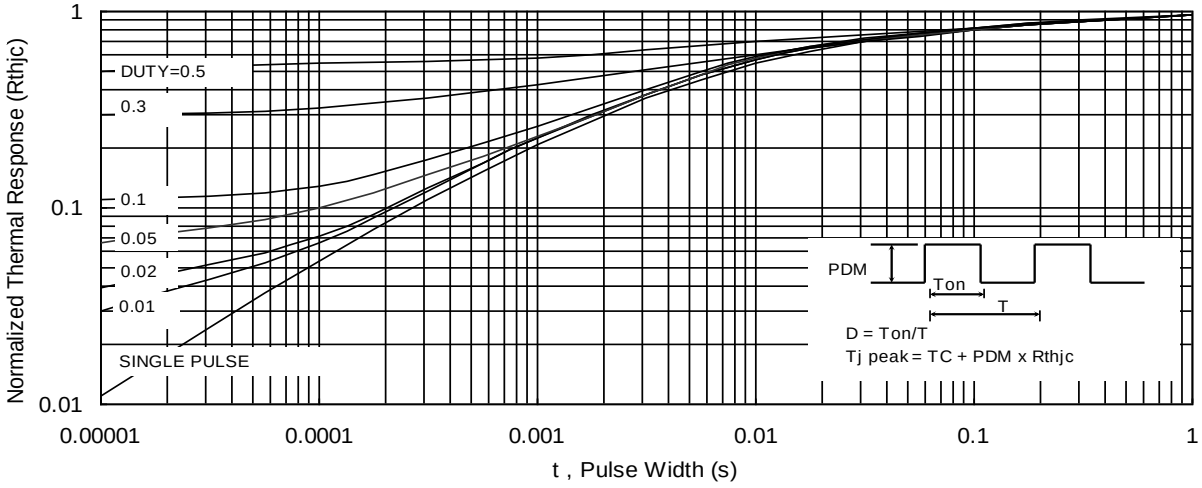


Fig.9 Normalized Maximum Transient Thermal Impedance

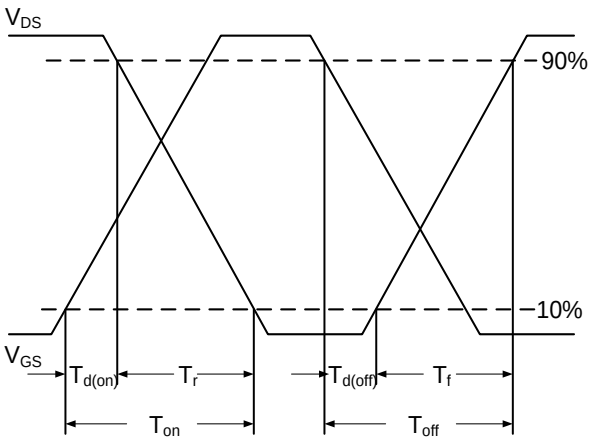


Fig.10 Switching Time Waveform

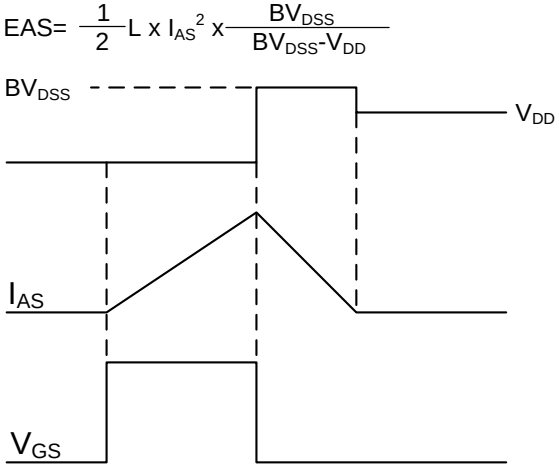


Fig.11 Unclamped Inductive Switching Wave

➢ P-Channel Typical Characteristics

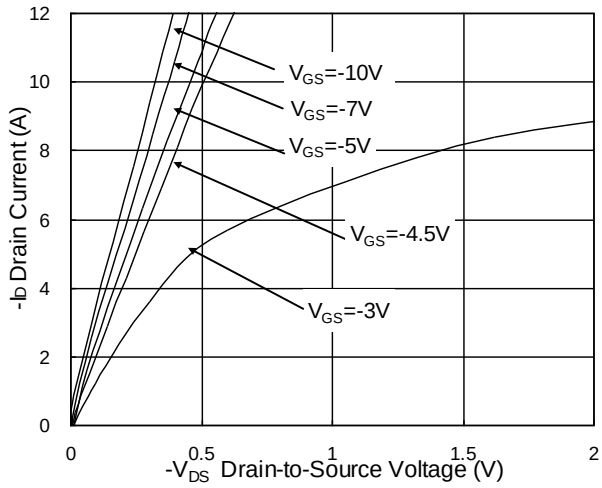


Fig.1 Typical Output Characteristics

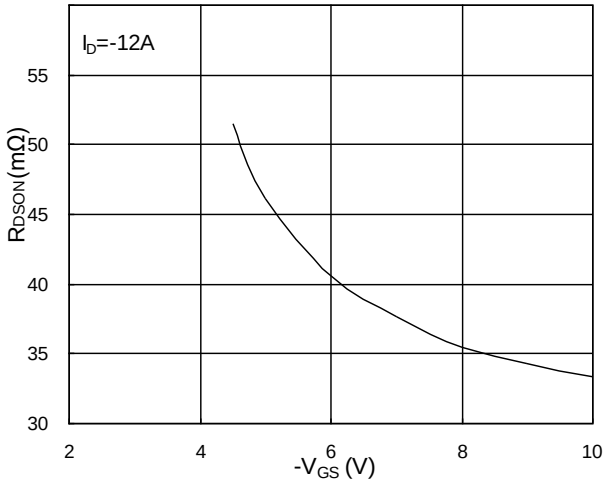


Fig.2 On-Resistance vs. G-S Voltage

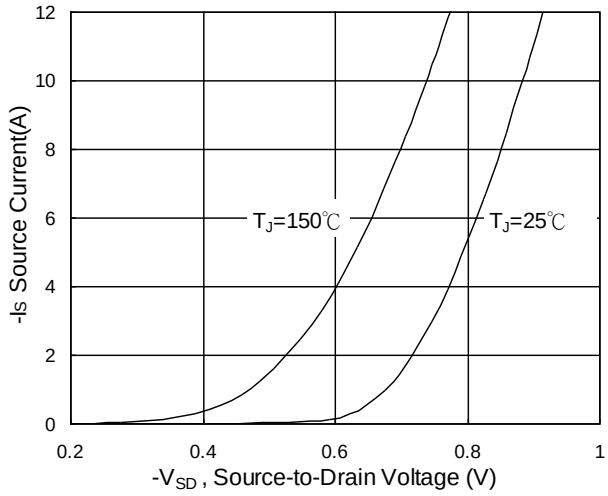


Fig.3 Source Drain Forward Characteristics

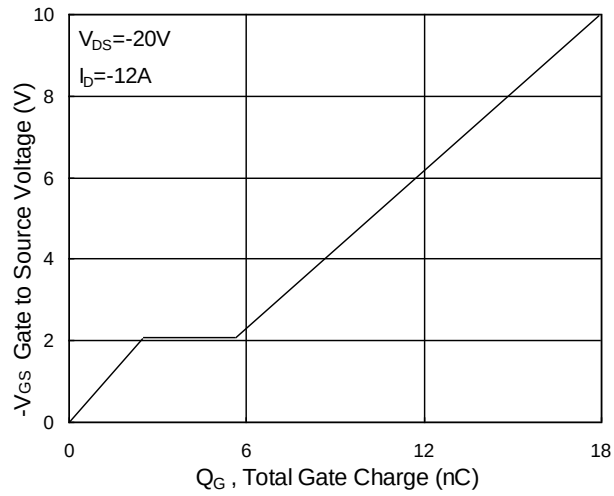


Fig.4 Gate-Charge Characteristics

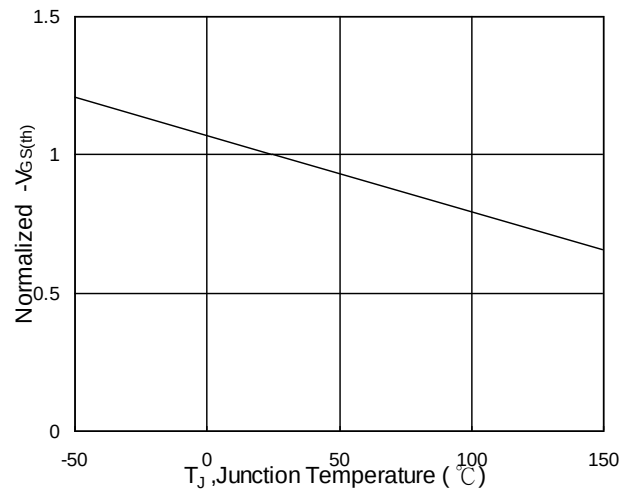


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

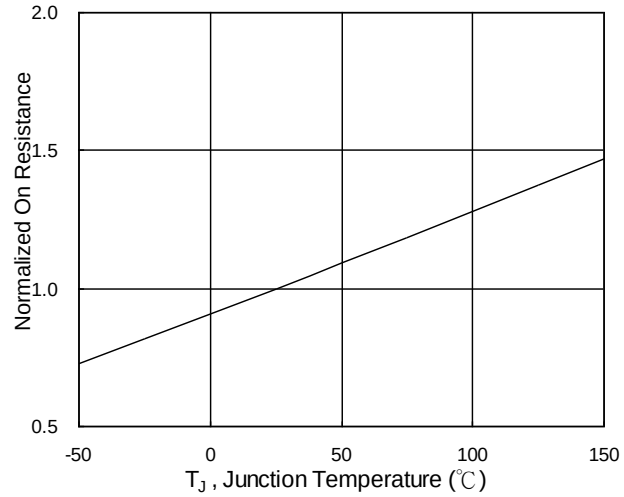


Fig.6 Normalized R_{DSON} vs. T_J

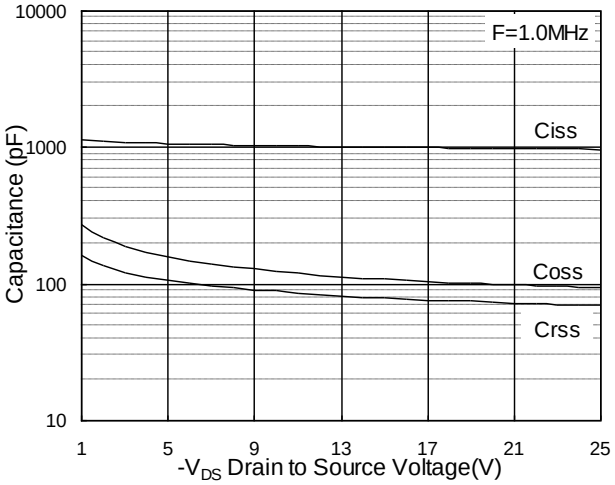


Fig.7 Capacitance

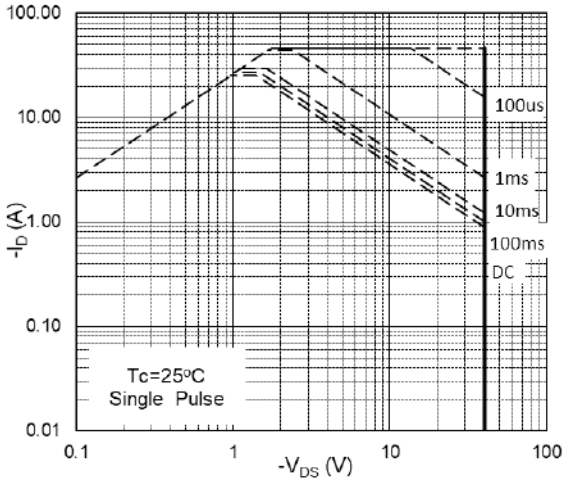


Fig.8 Safe Operating Area

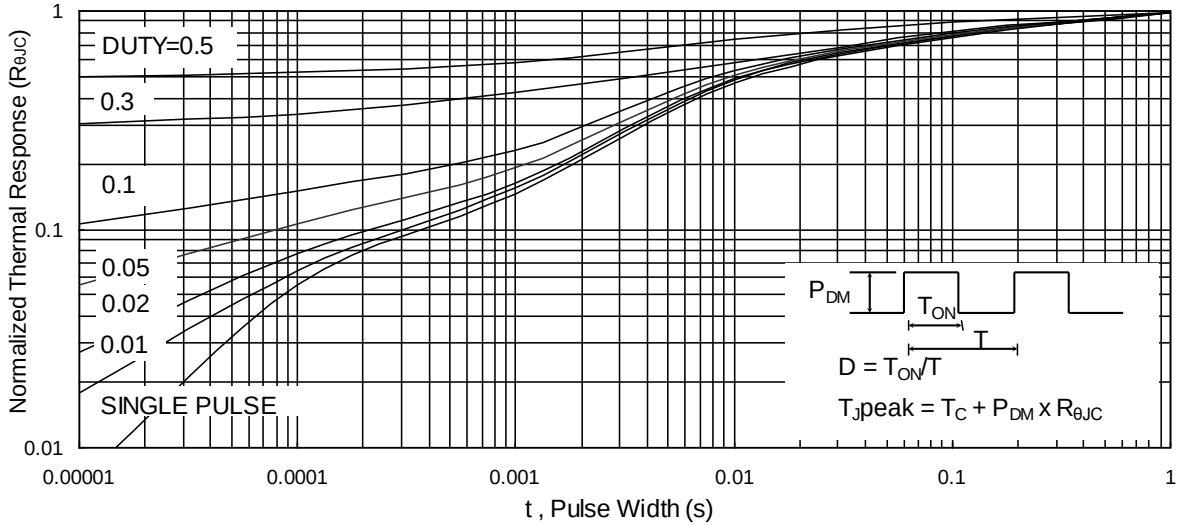
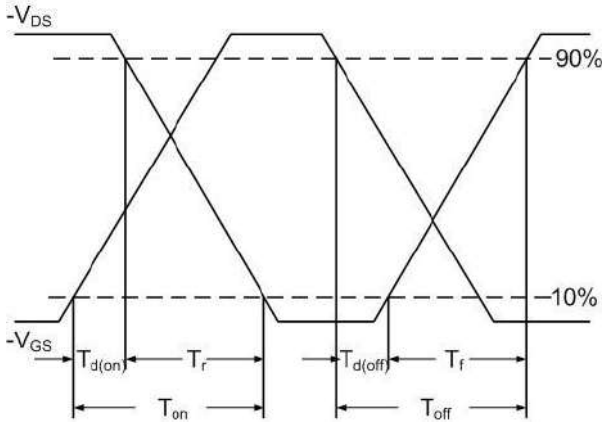


Fig.9 Normalized Maximum Transient Thermal Impedance



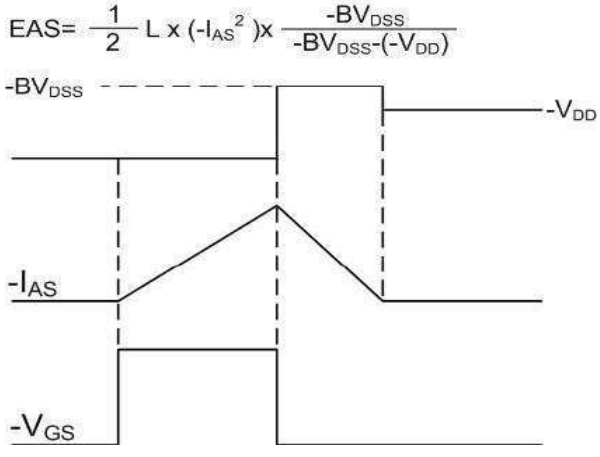
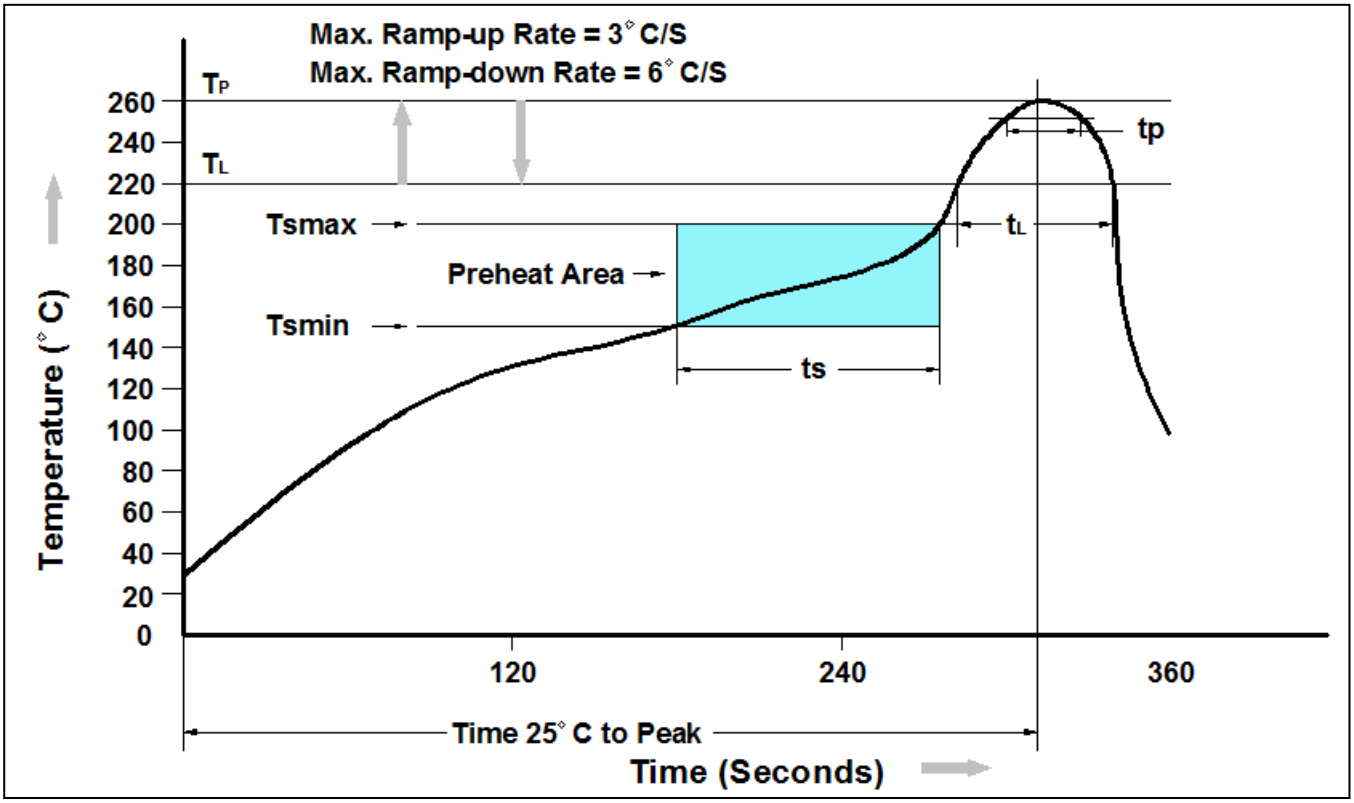


Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Waveform

➢ Recommand IR Reflow Soldering Thermal Profile

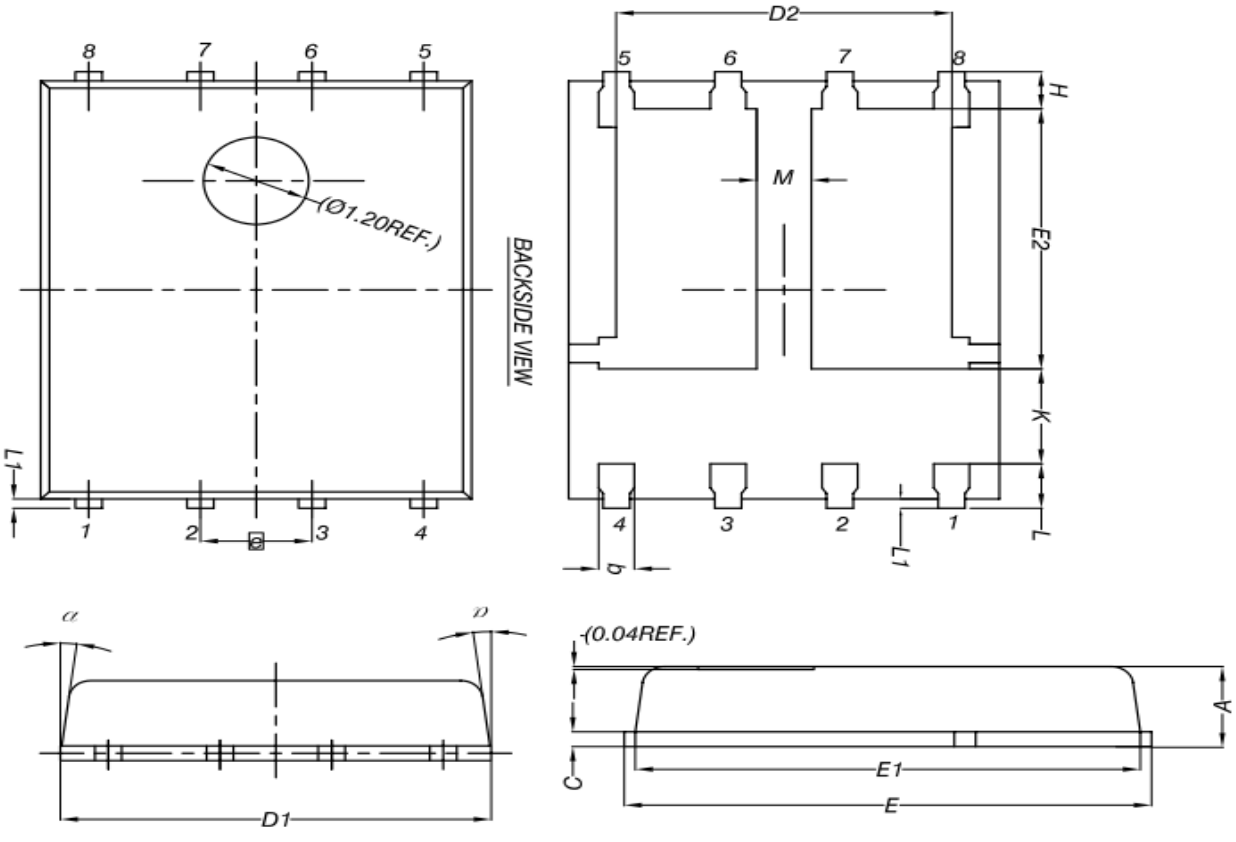


Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (ts) from (Tsmin to Tsmax)	60-120 seconds
Average Ramp-up Rate (tL to tP)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60 – 150 seconds
Peak Temperature	260°C +0°C / -5°C
Time (tP) within 5°C of actual Peak Temperature	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.

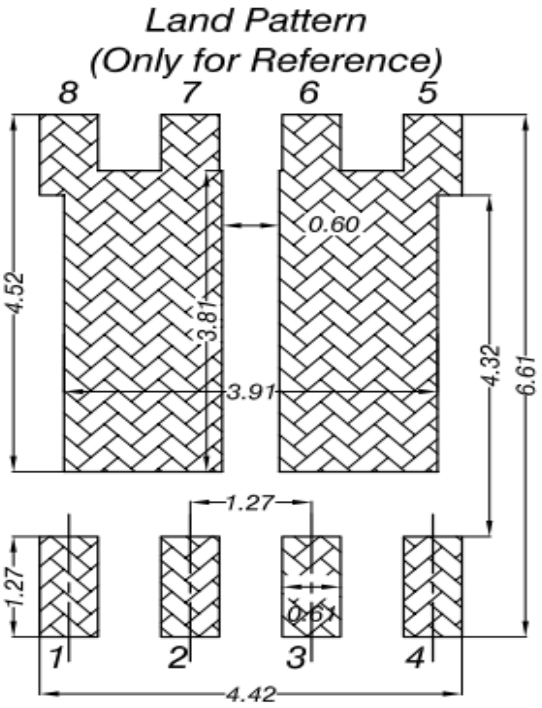
➢ Ordering Information

Part Number	Description	Quantity
PAC49TY03YB	DFN5X6A-EP2 Reel	3000 pcs

➢ Package Information (DFN5X6A-EP2)



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°



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